Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-18 (Cancelled).

Claim 19 (Previously Presented): A method of forming a semiconductor integrated circuit, the method comprising:

providing a substrate comprised of semiconductor material having isolation structures formed thereon, the substrate having a planarized surface exposing the semiconductor material of the substrate so that the isolation structures define exposed transistor forming regions of the substrate surface;

forming source and drain diffusion regions in exposed transistor forming regions of the substrate surface;

annealing the semiconductor substrate;

after forming the source and drain diffusion region and *after annealing*, covering the surface of the semiconductor substrate with a first layer of dielectric material to form a first interlayer dielectric layer on the semiconductor substrate after formation of the source and drain diffusions;

etching a gate electrode trench in the interlayer dielectric layer, the gate electrode trench configured for the placement of a transistor gate electrode between the source and drain regions, wherein etching the gate electrode trench in the first dielectric layer further includes forming a trench extension that extends into the substrate;

lining the gate electrode trench with a high-K dielectric film; and

depositing a gate electrode conductive material in the gate electrode trench after lining the trench with the high-K dielectric film.

Claim 20 (Previously Presented): The method as recited in claim 19 wherein the trench extension that extends into the substrate a depth sufficient to include an entire device inversion channel for the integrated circuit device.

Claim 21 (Previously Presented): The method as recited in claim 19 further comprising epitaxially growing a silicon layer in the trench extension.

Claim 22 (Previously Presented): The method as recited in claim 21 wherein the epitaxially grown silicon layer is a strained silicon layer formed on a SiGe layer grown in the channel trench.

Claim 23 (Previously Presented): The method as recited in claim 21 wherein the epitaxially grown silicon layer is a strained silicon layer formed on a Ge layer grown in the channel trench.

Claim 24 (Previously Presented): The method as recited in claim 21 wherein the epitaxially grown silicon layer is a strained silicon layer formed on one of a SiGe or Ge layer.

Claim 25 (Cancelled).

Claim 26 (Previously Presented): A method of forming a semiconductor integrated circuit, the method consisting of the following operations:

providing a substrate having isolation structures formed thereon so that the isolation structures define exposed transistor forming regions of the substrate surface;

forming source and drain diffusion regions in exposed transistor forming regions of the substrate surface;

annealing the semiconductor substrate;

performing post anneal processes including:

covering the surface of the semiconductor substrate with a first layer of dielectric material selected from among undoped silicate glass (USG) and phospho-silicate glass (PSG) to form a first interlayer dielectric layer on the semiconductor substrate after formation of the source and drain diffusions;

etching a gate electrode trench in the interlayer dielectric layer such that the trench extends into the substrate and so that the trench is configured for the placement of a transistor gate electrode between the source and drain regions;

lining walls of the gate electrode trench with a high-K dielectric film so that walls of the interlayer dielectric layer and walls of the trench extending into the substrate have the high-K dielectric film formed thereon;

forming a strained silicon channel in the gate electrode trench after lining the trench with the high-K dielectric film;

forming a conductive gate electrode in electrical contact with the strained silicon channel;

covering the surface of the semiconductor substrate with a second layer of dielectric material comprising a nitride layer forming a second interlayer dielectric layer on the semiconductor substrate after formation of the source and drain diffusions;

forming openings in the dielectric layers to expose source, drain, and gate regions; and

forming electrical contacts with the source and drain regions and the gate electrode.